L Numb r	Hits	Sear h T xt	DB	Tim stamp
1	64	(s rializer des rializer SERDES).ab. and (cl ck cl cking CLK) and (t st testing test d t ster)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 15:55
2	6	(serializer deserializer SERDES).ab. and (clock clocking CLK) and (test testing tested tester) and (test adj pattern)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 19:46
3	88	(serializer deserializer SERDES) and (clock clocking CLK) and (test testing tested tester) and (test adj pattern)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 16:07
4	36	(serializer deserializer SERDES) and (clock clocking CLK) and (test testing tested tester) and (test adj pattern) and (test with (serializer deserializer SERDES))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 15:56
5	36	(serializer deserializer SERDES or serializer?deserializer) and (clock clocking CLK) and (test testing tested tester) and (test adj pattern) and (test with (serializer deserializer SERDES))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 15:57
6	36	(serializer deserializer SERDES or serializer?deserializer) and (clock clocking CLK) and (test testing tested tester) and (test adj pattern) and (test with (serializer deserializer serializer?deserializer SERDES))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 15:57
7	3	(serializer deserializer SERDES or serializer?deserializer) and (clock clocking CLK) and (test testing tested tester) and (test adj pattern) and (test with (serializer deserializer serializer?deserializer SERDES)) and fpga	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 15:57
8	16	(serializer?deserializer SERDES) and (clock clocking CLK) and (test testing tested tester) and (test adj pattern)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 16:07
11	3	("5424655" | "5737235" | "5825201").PN.	USPAT	2004/02/04 16:11
14	0	6617877.URPN.	USPAT	2004/02/04 16:12
15	0	6617877.URPN.	USPAT	2004/02/04 16:12
16	0	6542096.URPN.	USPAT	2004/02/04 16:33

17	3	("5424655" | "5737235" | "5825201").PN.	USPAT	2004/02/04 16:35
18	0	6542096.URPN.	USPAT	2004/02/04 16:38
19	0	6542096.URPN.	USPAT	2004/02/04 16:38
20	0	6617877.URPN.	USPAT	2004/02/04 16:40
21	21	("5361373" "5537601" "5652904" "5671355" "5752035" "5970254" "6020755" "6096091" "6279045" "6282627" "6343207").pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 16:43
22	11	("5361373" "5537601" "5652904" "5671355" "5752035" "5970254" "6020755" "6096091" "6279045" "6282627" "6343207").pn.	USPAT	2004/02/04 16:43
33	517	fpga and Jitter	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 19:49
34	6	(fpga and Jitter).ab.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 19:52
35	1	6295315.pn.	USPAT	2004/02/04 19:52
-	2579	FPGA.ab.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 18:19
-	346	(serializer deserializer).ab.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 11:12
-	4	FPGA.ab. and ((serializer deserializer).ab.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 18:24
-	11	34363.pn. 5914616.pn. 5844829.pn. 6232845.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 18:25
-	8	("5790563" "5793822" "6003150" "6191614").pn.	USPAT; US-P PUB; EP ; JPO; DERWENT; IBM_TDB	2004/02/04 10:14

-	50	("5550843" "5675589" "5841790" "5844917" "5878051" "5237219" "5426738" "5426741" "5430687" "5508636" "5619513" "5651013" "5720031" "5732246" "5781756" "5848026" "5867507" "6021513" "6049487" "6134677" "6137738" "6150863" "6167001" "6173424" "6307877" "6321366" "6330693" "6331790" "6389379" "6421251" "6430088" "6436741" "6601218" "6631487" "5465261" "6141775" "6237021" "6239611" "5309428" "5363366" "5365513" "5381348" "5425017" "5444695" "5479355" "5633813" "5737693" "5841967" "5887244" "5898905").pn.	USPAT; US-PGPUB	2004/02/03 18:44

-	0	(("5550843" "5675589" "5841790" "5844917" "5878051" "5237219" "5426738" "5426741" "5430687" "5508636" "5619513" "5651013" "5720031" "5732246" "5781756" "5848026" "5867507" "6021513" "6049487" "6134677" "6137738" "6150863" "6167001" "6173424" "6307877" "6321366" "6330693" "6331790" "6389379" "6421251" "6430088" "6436741" "6601218" "6631487" "5465261" "6141775" "6237021" "6239611" "5309428" "5363366" "5365513" "5381348" "5425017" "5444695" "5479355" "5633813" "5737693" "5841967" "5887244" "5898905").pn.) and (("5790563" "5793822" "6003150" "6191614").pn.)	USPAT; US-PGPUB; EP ; JP ; DERWENT; IBM_TDB	2004/02/03 18:29

-	0	(("5550843" "5675589" "5841790" "5844917" "5878051" "5237219" "5426738" "5426741" "5430687" "5508636" "5619513" "5651013" "5720031" "5732246" "5781756" "5848026" "5867507" "6021513" "6049487" "6134677" "6137738" "6150863" "6167001" "6173424" "6307877" "6321366" "6330693" "6331790" "6389379" "6421251" "6430088" "6436741" "6601218" "6631487" "5465261" "6141775" "6237021" "6239611" "5309428" "5363366" "5365513" "5381348" "5425017" "5444695" "5479355" "5633813" "5737693" "5841967" "5887244" "5898905").pn.) and (34363.pn. 5914616.pn. 5844829.pn. 6232845.pn.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 18:29

-	0	(("5550843" "5675589" "5841790" "5844917" "5878051" "5237219" "5426738" "5426741" "5430687" "5508636" "5619513" "5651013" "5720031" "5732246" "5781756" "5848026" "5867507" "6021513" "6049487" "6134677" "6137738" "6150863" "6167001" "6173424" "6307877" "6321366" "6330693" "6331790" "6389379" "6421251" "6430088" "6436741" "6601218" "6631487" "5465261" "6141775" "6237021" "6239611" "5309428" "5363366" "5365513" "5381348" "5425017" "5444695" "5479355" "5633813" "5737693" "5841967" "5887244" "5898905").pn.) and (FP A.ab. and ((s rializer deserializer).ab.))	USPAT; US-PGPUB; EP ; JPO; DERWENT; IBM_TDB	2004/02/03 18:29

-	0	((serializ r deserializ r).ab.) and ((("5550843" "5675589" "5841790" "5844917" "5878051" "5237219" "5426738" "5426741" "5430687" "5508636" "5619513" "5651013" "5720031" "5732246" "5781756" "5848026" "5867507" "6021513" "6049487" "6134677" "6137738" "6150863" "6167001" "6173424" "6307877" "6321366" "6330693" "6331790" "6389379" "6421251" "6430088" "6436741" "6601218" "6631487" "5465261" "6141775" "6237021" "6239611" "5309428" "5363366" "5365513" "5381348" "5425017" "5444695" "5479355" "5633813" "5737693" "5841967" "5887244" "5898905").pn.)	USPAT; US-P PUB; EPO; JP ; DERWENT; IBM_TDB	2004/02/03 18:52

-	28971	((gate adj array) FP A)	USPAT; US-P PUB; EP ; JPO; DERWENT; IBM_TDB	2004/02/03 18:54
-	7207	((gate adj array) FPGA).ab.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 18:56
-	47	((gate adj array) FPGA).ab. and crc	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 19:03

-	49	("5550843" "5675589" "5841790" "5844917" "5878051" "5237219" "5426738" "5426741" "5430687" "5508636" "5619513" "5651013" "5720031" "5732246" "5781756" "5848026" "5867507" "6021513" "6049487" "6134677" "6137738" "6150863" "6167001" "6173424" "6307877" "6321366" "6330693" "6331790" "6389379" "6421251" "6430088" "6436741" "6601218" "6631487" "5465261" "6141775" "6237021" "6239611" "5309428" "5363366" "5365513" "5381348" "5425017" "5444695" "5479355" "5633813" "5737693" "5841967" "5887244" "5898905").pn. and fpga	USPAT; US-PGPUB	2004/02/03 19:03

-	8	"912683"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 11:12
-	366	(s rializ r d s rializer SERDES).ab.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 15:44
-	8	(serializer deserializer SERDES).ab. and (FPGA (gate adj array) PGA).ab.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/04 16:41

09912683_CLS
Most Frequently Occurring Classifications of Patents Returned
From A Search of 09912683 on October 28, 2003

Original Classifications

3	326/38
3	370/245
3	455/67.14
3	703/14
3	714/42
3	714/724
3	714/726
2	365/189.04
2	714/30

Cross-Reference Classifications

4	714/717
4	714/725
3	326/38
3	326/41
3	370/452
3	714/733
3	716/16
3	716/4
2	257/E23.124
2	257/E23.125
2	365/189.04
2	365/230.05
2	455/423
2	714/25
2	714/734

Combined Classifications

6	326/38
5	714/725
4	326/41
4	365/189.04
4	370/452
4	703/14
4	714/717
4	714/724
4	716/16
3	370/245
3	455/67.14
3	714/42
3	714/726
3	714/733
3	716/4

2 257/E23.124
2 257/E23.125
2 326/16
2 365/201
2 365/230.05
2 365/230.08
2 455/423
2 714/25
2 714/30
2 714/718
2 714/731
2 714/734
2 716/6

09912683_CLSTITLES

Titles of Most Frequently Occurring Classifications of Patents Returned

From A Search of 09912683 on October 28, 2003

6 326/38 (3 OR, 3 XR)
Class 326 : ELECTRONIC DIGITAL LOGIC CIRCUITRY
326/37 MULTIFUNCTIONAL OR PROGRAMMABLE (E.G., UNIVERSAL, ETC.)
326/38 .Having details of setting or programming of interconnections or logic functions

5 714/725 (1 OR, 4 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/724 .Digital logic testing
714/725 ..Programmable logic array (PLA) testing

4 326/41 (1 OR, 3 XR)
Class 326 : ELECTRONIC DIGITAL LOGIC CIRCUITRY
326/37 MULTIFUNCTIONAL OR PROGRAMMABLE (E.G., UNIVERSAL, ETC.)
326/39 .Array (e.g., PLA, PAL, PLD, etc.)
326/41 ..Significant integrated structure, layout, or layout interconnections

4 365/189.04 (2 OR, 2 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/189.01 READ/WRITE CIRCUIT
365/189.04 .Simultaneous operations (e.g., read/write)

4 370/452 (1 OR, 3 XR)
Class 370 : MULTIPLEX COMMUNICATIONS
370/431 CHANNEL ASSIGNMENT TECHNIQUES
370/449 .Polling
370/450 ..Passing a signal identifying the idle or busy state of a channel (e.g., token passing)
370/451 ...On bus
370/452 ....On ring or loop

4 703/14 (3 OR, 1 XR)
Class 703 : DATA PROCESSING: STRUCTURAL DESIGN, MODELING, SIMULATION, AND EMULATION
703/13 SIMULATING ELECTRONIC DEVICE OR ELECTRICAL SYSTEM
703/14 .Circuit simulation

4 714/717 (0 OR, 4 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/712 .Transmission facility testing
714/717 ..Loop or ring configuration

4 714/724 (3 OR, 1 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/724 .Digital logic testing

4 716/16 (1 OR, 3 XR)
Class 716 : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
716/1 CIRCUIT DESIGN
716/12 .Routing (e.g., routing map, netlisting)
716/16 ..PLA, PLD, FPGA, OR MCM

3 370/245 (3 OR, 0 XR)
Class 370 : MULTIPLEX COMMUNICATIONS
370/241 DIAGNOSTIC TESTING (OTHER THAN SYNCHRONIZATION
)

370/242 .Fault detection
370/245 ..Of a local area network

3 455/67.14 (3 OR, 0 XR)
Class 455 : TELECOMMUNICATIONS
455/39 TRANSMITTER AND RECEIVER AT SEPARATE STATIONS

455/67.11 .Having measuring, testing, or monitoring of system or part
455/67.14 ..Using a test signal

3 714/42 (3 OR, 0 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/100 DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING

714/1 .Reliability and availability
714/25 ..Fault locating (i.e., diagnosis or testing)

714/40 ...Component dependent technique
714/42 ....Memory or storage device component fault

3 714/726 (3 OR, 0 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/724 .Digital logic testing
714/726 ..Scan path testing (e.g., level sensitive scan design (LSSD))

3 714/733 (0 OR, 3 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/724 .Digital logic testing
714/733 ..Built-in testing circuit (BILBO)

3 716/4 (0 OR, 3 XR)
Class 716 : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
716/1 CIRCUIT DESIGN
716/4 .Testing or evaluating

2 257/E23.124 (0 OR, 2 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/E23.113 ....Ceramic materials or glass (EPO)
257/E23.116 .Encapsulations, e.g., encapsulating layers, coatings, e.g., for protection (EPO)
257/E23.123 ..Characterized by arrangement or shape (EPO)
257/E23.124 ...Device being completely enclosed (EPO)

2 257/E23.125 (0 OR, 2 XR)
Class 257 : ACTIVE SOLID-STATE DEVICES
257/E23.113 ....Ceramic materials or glass (EPO)
257/E23.116 .Encapsulations, e.g., encapsulating layers, coatings, e.g., for protection (EPO)
257/E23.123 ..Characterized by arrangement or shape (EPO)
257/E23.124 ...Device being completely enclosed (EPO)
257/E23.125 ....Substrate forming part of encapsulation (EPO)

2 326/16 (1 OR, 1 XR)
Class 326 : ELECTRONIC DIGITAL LOGIC CIRCUITRY
326/16 WITH TEST FACILITATING FEATURE

2 365/201 (1 OR, 1 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL

365/189.01 READ/WRITE CIRCUIT
365/201 .Testing

2 365/230.05 (0 OR, 2 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/230.01 ADDRESSING
365/230.05 .Multiple port access

2 365/230.08 (1 OR, 1 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/230.01 ADDRESSING
365/230.08 .Including particular address buffer or latch circuit arrangement

2 455/423 (0 OR, 2 XR)
Class 455 : TELECOMMUNICATIONS
455/403 RADIOTELEPHONE SYSTEM
455/422.1 .Zoned or cellular telephone system
455/423 ..Diagnostic testing, malfunction indication, or electrical condition measurement

2 714/25 (0 OR, 2 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/100 DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING

714/1 .Reliability and availability
714/25 ..Fault locating (i.e., diagnosis or testing)

2 714/30 (2 OR, 0 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/100 DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING

714/1 .Reliability and availability
714/25 ..Fault locating (i.e., diagnosis or testing)

714/27 ...Particular access structure
714/30 ....Built-in hardware for diagnosing or testing within-system component (e.g., microprocessor test mode circuit, scan path)

2 714/718 (1 OR, 1 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY

09912683_CLSTITLES

714/699 PULSE OR DATA ERROR HANDLING
714/718 .Memory testing

2 714/731 (1 OR, 1 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/724 .Digital logic testing
714/726 ..Scan path testing (e.g., level sensitive scan design (LSSD))
714/731 ...Clock or synchronization

2 714/734 (0 OR, 2 XR)
Class 714 : ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY
714/699 PULSE OR DATA ERROR HANDLING
714/724 .Digital logic testing
714/734 ..Structural (in-circuit test)

2 716/6 (1 OR, 1 XR)
Class 716 : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
716/1 CIRCUIT DESIGN
716/4 .Testing or evaluating
716/5 ..Design verification (e.g., wiring line capacitance, fan-out checking, minimum path width)
716/6 ...Timing analysis (e.g., delay time, path delay, latch timing)

09912683_LIST

PLUS Search Results for S/N 09912683, Searched October 28, 2003

5550843
5675589
5841790
5844917
5878051
5237219
5426738
5426741
5430687
5508636
5619513
5651013
5720031
5732246
5781756
5848026
5867507
6021513
6049487
6134677
6137738
6150863
6167001
6173424
6307877
6321366
6330693
6331790
6389379
6421251
6430088
6436741
6601218
6631487
5465261
6141775
6237021
6239611
5309428
5363366
5365513
5381348
5425017
5444695
5479355
5633813

09912683_LIST

5737693
5841967
5887244
5898905

5550843 62
5675589 62
5841790 62
5844917 62
5878051 62
5237219 62
5426738 62
5426741 62
5430687 62
5508636 62
5619513 62
5651013 62
5720031 62
5732246 62
5781756 62
5848026 62
5867507 62
6021513 62
6049487 62
6134677 62
6137738 62
6150863 62
6167001 62
6173424 62
6307877 62
6321366 62
6330693 62
6331790 62
6389379 62
6421251 62
6430088 62
6436741 62
6601218 62
6631487 62
5465261 60
6141775 51
6237021 51
6239611 51
5309428 51
5363366 51
5365513 51
5381348 51
5425017 51
5444695 51
5479355 51
5633813 51
5737693 51
5841967 51

5887244 51
5898905 51